Remarks

Claims 1-18 were canceled in previous responses. Claims 19-34 stand rejected. Claims 24-26, 30 and 34 are canceled herein; thus, claims 19-23, 27-29 and 31-33 remain pending. Claims 19, 20, 23, 27, 28, 31 and 33 are amended herein. The Applicant respectfully traverses the rejection and requests allowance of claims 19-23, 27-29 and 31-33.

Claim Amendments

Independent claim 19 is amended to incorporate the subject matter of claim 30. As a result, amended claim 19 now provides for the processing of instruction bundles for *two* separate threads in each of the clusters of execution units. The labeling of each bundle and thread (e.g., first, second, etc.) has also been altered in conjunction with the amendments. Independent claim 31 is amended in a similar fashion by incorporating the subject matter of claim 34. As a result, claims 30 and 34 are canceled herein.

Claims 20, 27 and 33 are amended to align the language of those claims with the amendments to independent claims 19 and 31. Claim 33 is further amended to correct a typographical error involving the word "data."

Claim 23 is amended to further address the fetching step for each of the six bundles cited in claim 19. As this amendment incorporates the subject matter of claims 24-26, these claims are canceled herein.

Claims 28 and 33 are amended to indicate that a latch is used to bypass data between a register file of the first cluster and a register file of the second cluster. Support for this amendment is provided in the present application at Fig. 5, in which either latch 314 or latch 316 is positioned between register files 304A, 304B of the processing cores 302A, 302B.

Claim Rejection Under 35 U.S.C. § 102

Claims 19-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,272,616 to Fernando et al. (hereinafter "Fernando"). (Page 2 of the Office action.) The Applicant respectfully traverses the rejection in light of the current amendments to the claims, and in view of the following discussion.

Claims 19 and 31

Amended independent method claim 19 now indicates that a bundle of instructions from each of first and second program threads are distributed to a first cluster of execution units for execution, while a bundle from each of third and fourth program threads are distributed to a second cluster of execution units in throughput mode. In other words, during throughput mode, each of the clusters receives instructions from more than one thread. Amended processor claim 31 incorporates similar provisions. Paragraph [0019] of the present application describes such execution in one embodiment as "maximum throughput of four separate threads."

With respect to former claim 30, the Office action indicates that Fernando teaches such operation by way of its MIMD mode. (Pages 11-13 of the Office action.) The Applicant respectfully disagrees, as the MIMD mode of Fernando appears to only teach the receipt and execution of instructions from a single program thread or stream at each of the instruction pipelines. For example, Fig. 7, which indicates the use of four instruction pipelines, shows threads 1 through 4 each being executed on separate instruction pipelines while in MIMD mode at time t1 through t9. (See column 11, lines 33-60.) At time t10 through t12, instruction pipelines 1 and 2 operate in SIMD mode, while instruction pipeline 4 operates in MIMD mode on thread 4. (See column 11, line 60, to column 12, line 4.) Thus, the Applicant contends that Fernando does not teach or suggest two clusters, each of which receive instruction bundles from two separate program threads while in throughput mode, as provided for in claims 19 and 31, and such indication is respectfully requested.

Claims 20-23, 27-29, 32 and 33

Claims 20-23 and 27-29 depend from independent claim 19, while claims 32 and 33 depend from independent claim 31, thus incorporating the provisions of their respective independent claims. Thus, the Applicant asserts that claims 20-23, 27-29, 32 and 33 are allowable for at least the reasons provided above in support of claims 19 and 31, and such indication is respectfully requested.

Further regarding amended claims 28 and 33, the Office action appears to indicate that the register files 25 of each of the instruction pipelines 16, 18 teach the latch of claims 28 and 33. (Please see pages 10 and 11 of the Office action.) The Applicant respectfully disagrees in light of the current amendments to claims 28 and 33, as the latch recited therein resides *between*

register files, and thus is not a constituent of either register file or cluster. Such a latch 314, 316 is shown in the present application at Fig. 5, depicted separately from the register files 304A, 304B associated with separate processing cores 302A, 302B. Oppositely, Fernando only discloses a register *bus* 38 between the register files 25, with its register files 25 located *within* the data path 24 of each of the instruction pipelines 16, 18. Further, Fernando does not appear to indicate a separate latch associated with the register bus 38. Thus, the Applicant contends that amended claims 28 and 33 are allowable in view of Fernando for at least these additional reasons, and such indication is respectfully requested.

Claims 24-26, 30 and 34

Claims 24-26, 30 and 34 are canceled herein, thus obviating the rejection as it pertains to these claims.

Therefore, in light of the foregoing, the Applicant respectfully requests the withdrawal of the 35 U.S.C. § 102 rejection of claims 19-34.
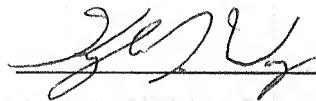
Conclusion

Based on the above remarks, the Applicant submits that claims 19-23, 27-29 and 31-33 are allowable. Additional reasons in support of patentability exist, but such reasons are omitted in the interests of clarity and brevity. The Applicant thus respectfully requests allowance of claims 19-23, 27-29 and 31-33.

The Applicant believes no fees are due with respect to this filing. However, should the Office determine additional fees are necessary, the Office is hereby authorized to charge Deposit Account No. 08-2025 accordingly.

Respectfully submitted,

Date: 7 / 9 / 2007

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